CKGEN IP SPEC

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## Introduction

The CKGEN module is used to generate clocks for digital part of the chip.

## Feature

Consist of CKGEN1 and CKGEN2.

Sub-module CKGEN1 generates clocks for normal logic.

Sub-module CKGEN2 generates clocks for safety requirements.

## Functional Details

### Block Diagram

The following diagram shows the main inputs and outputs of CKGEN.



Figure1 CKGEN diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| CLK\_256K\_SC | O | 1 | Scan-muxed CLK\_256K | 1.952us(50% duty) |
| CLK\_32M\_SC | O | 1 | Scan\_muxed CLK\_32M | 15.625ns |
| CLK\_32M\_EN | O | 1 | Real gate for CLK\_32M | Level(CLK\_32M domain) |
| CLK\_32M\_ORG\_SC | O | 1 | Scan\_muxed original CLK\_32M | 15.625ns |
| CLK\_OUT\_SC | O | 1 | Scan\_muxed CLK\_OUT | 15.625ns or 1.952us |
| CLK\_8M\_256K\_SC | O | 1 | Scan\_muxed CLK\_8M\_256K | 15.625ns or 62.5ns |
| CLK\_REG\_SC | O | 1 | Scan\_muxed CLK\_REG | 62.5ns |
| CLK\_REG | O | 1 | 8MHz divided from CLK\_32M | 62.5ns |
| pulse\_2M | O | 1 | 2MHz pulse divided from CLK\_32M | 125ns |
| pulse\_1M | O | 1 | 1MHz pulse divided from CLK\_32M | 125ns |
| ADC\_CLK\_H | O | 1 | 2 timers frequency clock of ADC\_CLK |  |
| ADC\_CLK | O | 1 | Clock set by ADC\_CLK\_SET[1:0] |  |
| CLK\_ADC\_SC | O | 1 | Scan\_muxed ADC\_CLK\_H |  |
| AUX\_ADC\_CLK\_H | O | 1 | 2 timers frequency clock of ADC\_AUX\_CLK |  |
| AUX\_ADC\_CLK | O | 1 | Clock set by ADC\_CLK\_SET[1:0] |  |
| CLK\_AUX\_ADC\_SC | O | 1 | Scan\_muxed AUX\_ADC\_CLK\_H |  |
| CLK\_I2C\_SC | O | 1 | Gated CLK\_400K\_SC by I2C\_MAS\_EN |  |
| CLK\_MTP\_SC | O | 1 | Gated CLK\_400K\_SC by MTP\_EN |  |
| CLK\_CB\_SC | O | 1 | Gated CLK\_SLOW\_SC by CB\_EN |  |
| CLK\_SLOW\_SC | O | 1 | Scan\_muxed CLK\_SLOW |  |
| CLK\_SLOW2\_SC | O | 1 | Scan\_muxed CLK\_SLOW2 |  |
| pulse\_SLOW2\_2ms | O | 1 | 2ms period pulse divided from CLK\_SLOW2\_SC | 3.9us |
| resetb\_CLK | I | 1 | Asynchronous reset signal(synchronously released) | Level(CLK\_32M domain) |
| resetb\_CLK\_256K | I | 1 | Asynchronous reset signal(synchronously released by CLK\_256K) | Level(CLK\_256K domain) |
| resetb\_SR\_CLK\_SLOW | I | 1 | Scan\_muxed resetb and soft resetb for CLK\_SLOW domain | Level |
| SCAN\_MODE | I | 1 | For DFT test |  |
| SCAN\_CLK | I | 1 | Clock for DFT test |  |
| CLK\_32M | I | 1 | Main clock. When A2D\_SLEEP\_1P8 high, after 4us, CLK\_32M is off | 31.25ns period |
| CLK\_256K | I | 1 | Always on low clock | 3.90625us period |
| CLK\_32M\_OK | I | 1 | CLK\_32M\_OK high means CLK\_32M is accurate and can be used |  |
| ADC\_CLK\_SET | I | 2 | From reg, ADC clock selection | Level(CLK\_REG domain) |
| CB\_EN | I | 1 | From reg, Cell balance enable | Level(CLK\_REG domain) |
| D2A\_CELL\_ADC\_EN | I | 1 | CELL\_ADC enable | Level(CLK\_REG domain) |
| D2A\_AUX\_ADC\_EN | I | 1 | AUX\_ADC enable | Level(CLK\_REG domain) |
| SOFT\_RSTB\_REG | I | 1 | From reg, soft reset (low reset) | Level(CLK\_REG domain) |
| I2C\_MAS\_EN | I | 1 | I2C\_MAS enable | Level(CLK\_REG domain) |
| MTP\_EN | I | 1 | MTP interface enable | Level(CLK\_REG domain) |

### Clock Definition

The following table describes clocks defined in Figure 1 clock block diagram and other sections of this document.

|  |  |
| --- | --- |
| Clock Name | Definition |
| CLK\_32M\_SC | For u\_BASIC\_CTRL |
| CLK\_REG\_SC | For u\_COMM\_CTRL, u\_FRAME\_COUNTER, u\_COMM\_TO, u\_COMM\_REG |
| ADC\_CLK | For analog part |
| ADC\_CLK\_H | For analog part |
| AUX\_ADC\_CLK | For analog part |
| AUX\_ADC\_CLK\_H | For analog part |
| CLK\_ADC\_SC | For u\_ADC\_CTRL |
| CLK\_AUX\_ADC\_SC | For u\_AUX\_ADC\_CTRL |
| CLK\_I2C\_SC | For u\_I2C\_MAS |
| CLK\_MTP\_SC | For u\_MTP\_TOP |
| CLK\_CB\_SC | For u\_CB\_CTRL |
| CLK\_SLOW\_SC | For u\_CYC\_WAKE, u\_OVUV\_OTUT\_CMP, u\_FLT\_LOGIC, u\_TO\_SLP\_sync, u\_TO\_SD\_sync, u\_SOFT\_RSTB\_sync |
| CLK\_SLOW2\_SC | For u\_GAP\_CMP, u\_CONF\_REG\_CRC\_DET, u\_MTP\_REG\_CRC\_DET |
| CLK\_OUT\_SC | For u\_DS\_BASIC |
| CLK\_8M\_256K\_SC | For u\_CB\_CTRL, u\_FLT\_REG |

Table1 clock definitions

### CKGEN function description

The following diagram shows the clock architecture and various clock sources for this chip.

Figure2 clock diagram(HWR003/004/005/006/007\_CKGEN1)



Figure3 CLK\_SWITCH diagram

#### CLK\_32M\_SC

When CLK\_32M\_OK turns high from low, CLK\_32M is stable.

When CLK\_32M\_OK turns high from low, CLK\_32M is still useable within 4us.

Thus ON\_32M is generated. ON\_32M’s posedge is 1 clock later than CLK\_32M\_OK, but its negedge is 4us later than CLK\_32M\_OK.

CLK\_32M\_DGL is the gated clock of CLK\_32M, gated by ON\_32M.

CLK\_32M\_SC is the scan-muxed result of CLK\_32M\_DGL.

#### CLK\_REG\_SC

8MHz clock divided form CLK\_32M\_SC. (HWR006\_CKGEN1)

#### ADC\_CLK, ADC\_CLK\_H

(HWR007\_CKGEN1)

ADC\_CLK freq setting：ADC\_CLK\_SET[1:0]

2'b00 : ADC\_CLK 250k

2'b01: ADC\_CLK 500k

2'b10 : ADC\_CLK 1M

2'b11 : ADC\_CLK 1.5M

Frequency of ADC\_CLK\_H is 2 times of ADC\_CLK with 7/16 duty.

#### AUX\_ADC\_CLK,AUX\_ ADC\_CLK\_H

(HWSR003\_CKGEN2)

AUX\_ADC\_CLK freq setting：ADC\_CLK\_SET[1:0]

2'b00 : ADC\_CLK 250k

2'b01: ADC\_CLK 500k

2'b10 : ADC\_CLK 1M

2'b11 : ADC\_CLK 1.5M

Frequency of AUX\_ADC\_CLK\_H is 2 times of ADC\_CLK with 7/16 duty.

#### CLK\_ADC\_SC

Scan-muxed result of ADC\_CLK\_H. (HWSR001/002\_CKGEN2)

#### CLK\_AUX\_ADC\_SC

Scan-muxed result of AUX\_ADC\_CLK\_H.

#### CLK\_I2C\_SC

CLK\_400K is the divided clock of CLK\_32M, divided by 80.

CLK\_400K\_SC is the scan-muxed result of CLK\_400K.

CLK\_I2C\_SC is the gated clock of CLK\_400K\_SC, gated by I2C\_MAS\_EN.(HWR004\_CKGEN1)

#### CLK\_MTP\_SC

CLK\_MTP\_SC is the gated clock of CLK\_400K\_SC, gated by MTP\_EN. (HWR004\_CKGEN1)

#### CLK\_OUT\_SC

(HWR001\_CKGEN1)

When ON\_32M is high, CLK\_OUT is from CLK\_32M.

When ON\_32M is low, CLK\_OUT is from CLK\_256K.

Glitch-free logic is used for CLK\_OUT.

CLK\_OUT\_SC is the scan-muxed result of CLK\_OUT.

#### CLK\_8M\_256K\_SC

When ON\_32M is high, CLK\_8M\_256K is from CLK\_REG.

When ON\_32M is low, CLK\_8M\_256K is from CLK\_OUT.

Glitch-free logic is used for CLK\_8M\_256K.

CLK\_8M\_256K\_SC is the scan-muxed result of CLK\_8M\_256K.

#### CLK\_SLOW\_SC

(HWR001\_CKGEN1)

Pulse\_256K is the divided signal CLK\_32M, divided by 125, with duty 1/125.

When ON\_32M is high, CLK\_SLOW is from pulse\_125K.

When ON\_32M is low, CLK\_SLOW is from CLK\_OUT(from CLK\_256K).

CLK\_SLOW\_SC is the scan-muxed result of CLK\_SLOW.

#### CLK\_SLOW2\_SC

(HWSR001/002\_CKGEN2)

Redundant copy of CLK\_SLOW\_SC for safety use, using separate path with CLK\_SLOW\_SC.

#### CLK\_CB\_SC

CLK\_CB\_SC is the gated clock of CLK\_SLOW\_SC, gated by CB\_EN. (HWR004\_CKGEN1)

#### Operating Modes

To save power, most of clock source can be gated in low power mode.

The following table shows the clock availability in low power modes.

| **Clock Name** | **Sleep** | **active** | **shutdown** |
| --- | --- | --- | --- |
| CLK\_32M\_SC | No  (by ON\_32M) | Yes | No |
| CLK\_REG\_SC | No  (by ON\_32M) | Yes | No |
| ADC\_CLK | No  (by D2A\_CELL\_ADC\_EN) | Yes  (by D2A\_CELL\_ADC\_EN) | No |
| ADC\_CLK\_H | No  (by D2A\_CELL\_ADC\_EN) | Yes  (by D2A\_CELL\_ADC\_EN) | No |
| AUX\_ADC\_CLK | No  (by D2A\_AUX\_ADC\_EN) | Yes  (by D2A\_AUX\_ADC\_EN) | No |
| AUX\_ADC\_CLK\_H | No  (by D2A\_AUX\_ADC\_EN) | Yes  (by D2A\_AUX\_ADC\_EN) | No |
| CLK\_ADC\_SC | No  (by D2A\_CELL\_ADC\_EN) | Yes  (by D2A\_CELL\_ADC\_EN) | No |
| CLK\_AUX\_ADC\_SC | No  (by D2A\_AUX\_ADC\_EN) | Yes  (by D2A\_AUX\_ADC\_EN) | No |
| CLK\_I2C\_SC | No  (by I2C\_MAS\_EN) | Yes  (by I2C\_MAS\_EN) | No |
| CLK\_MTP\_SC | No  (by MTP\_EN) | Yes  (by MTP\_EN) | No |
| CLK\_CB\_SC | Yes  (by CB\_EN) | Yes  (by CB\_EN) | No |
| CLK\_SLOW\_SC | Yes  (from CLK\_256K) | Yes  (from pulse\_125K) | No |
| CLK\_OUT\_SC | Yes  (from CLK\_256K) | Yes  (from CLK\_32M) | No |

Table 2 clock availability in different modes